

CLAIMS

What is claimed is:

- 1 1. A cell protection circuit, comprising:
2 a transistor coupled to said cell; and
3 a current bypass device coupled to said transistor and said cell;
4 wherein said transistor limits the current that can flow through said cell when the voltage
5 across said cell falls to a predetermined minimum level.
- 1 2. The cell protection circuit of claim 1 wherein said current bypass device conducts current
2 when said transistor limits the current through the cell.
- 1 3. The cell protection circuit of claim 1 wherein said transistor is connected in series with said
2 cell and said current bypass device is connected in parallel to said serially connected transistor and
3 cell.
- 1 4. The cell protection circuit of claim 1 wherein said current bypass device comprises a diode.
- 1 5. The cell protection circuit of claim 1 wherein said transistor comprises a MOSFET.
- 1 6. The cell protection circuit of claim 1 wherein said transistor comprises an n-channel
2 enhancement mode MOSFET.

1 7. The cell protection circuit of claim 6 wherein the n-channel enhancement mode MOSFET
2 has a threshold voltage substantially the same as the predetermined minimum level.

1 8. The cell protection circuit of claim 7 wherein said current bypass device comprises a diode.

1 9. The cell protection circuit of claim 8 wherein said n-channel enhancement mode MOSFET
2 has gate, source and drain terminals and said source terminal couples to the negative terminal of
3 said cell, said drain terminal couples to the anode of said diode, and the cathode of said diode and
4 said gate terminal couple to the positive terminal of said cell.

1 10. The cell protection circuit of claim 1 wherein said transistor comprises an p-channel
2 enhancement mode MOSFET.

1 11. The cell protection circuit of claim 10 wherein the p-channel enhancement mode MOSFET
2 has a threshold voltage substantially the same as the predetermined minimum level.

1 12. The cell protection circuit of claim 11 wherein said current bypass device comprises a
2 diode.

1 13. The cell protection circuit of claim 12 wherein said p-channel enhancement mode
2 MOSFET has gate, source and drain terminals and said source terminal couples to the positive
3 terminal of said cell, said drain terminal couples to the cathode of said diode, and the anode of said
4 diode and said gate terminal couple to the negative terminal of said cell.

1 14. The cell protection circuit of claim 1 further including a delay device coupled to said cell
2 and said transistor, said delay device slows the rate of change of voltage across said cell with
3 changes in current load on said cell.

1 15. The cell protection circuit of claim 14 wherein said delay device comprises a resistor
2 coupled to a capacitor.

1 16. A protection circuit for a cell, comprising:
2 a means for limiting current through said cell when the voltage across said cell reaches a
3 predetermined threshold; and
4 a means for conducting current around said cell when the voltage across said cell reaches
5 the predetermined threshold.

1 17. The protection circuit of claim 16 further including a means for providing a time delay.

1 18. A method of protecting a cell, comprising:
2 (a) limiting the current said cell when the voltage across said cell falls to a minimum
3 predetermined level; and
4 (b) when limiting the current, permitting current to conduct through a bypass device
5 coupled in parallel with said cell.

1 19. The method of claim 18 wherein (a) is performed using a transistor.

1 20. The method of protecting a cell further including providing a time delay to the voltage
2 across said transistor.

1 21. A battery, comprising:
2 a plurality of cells connected in series; and
3 a separate protection unit coupled to each cell, each protection unit protecting its associated
4 cell and comprising:
5 a transistor coupled to said associated cell; and
6 a current bypass device coupled to said transistor and said associated cell;
7 wherein said transistor limits the current that can flow through said associated cell
8 when the voltage across said associated cell falls to a predetermined
9 minimum level.

1 22. The battery of claim 21 wherein said current bypass device conducts current when said
2 transistor limits the current through the cell.

1 23. The battery of claim 21 wherein said transistor is connected in series with said cell and said
2 current bypass device is connected in parallel to said serially connected transistor and cell.

1 24. The battery of claim 21 wherein said current bypass device comprises a diode.

1 25. The battery of claim 21 wherein said transistor comprises a MOSFET.

1 26. The battery of claim 21 wherein said transistor comprises an n-channel enhancement mode
2 MOSFET.

1 27. The battery of claim 26 wherein the n-channel enhancement mode MOSFET has a
2 threshold voltage substantially the same as the predetermined minimum level.

1 28. The battery of claim 27 wherein said current bypass device comprises a diode.

1 29. The battery of claim 28 wherein said n-channel enhancement mode MOSFET has gate,
2 source and drain terminals and said source terminal couples to the negative terminal of said cell,
3 said drain terminal couples to the anode of said diode, and the cathode of said diode and said gate
4 terminal couple to the positive terminal of said cell.

1 30. The battery of claim 21 wherein said transistor comprises an p-channel enhancement mode
2 MOSFET.

1 31. The battery of claim 30 wherein the p-channel enhancement mode MOSFET has a
2 threshold voltage substantially the same as the predetermined minimum level.

1 32. The battery of claim 31 wherein said current bypass device comprises a diode.

1 33. The battery of claim 32 wherein said p-channel enhancement mode MOSFET has gate,
2 source and drain terminals and said source terminal couples to the positive terminal of said cell,

3 said drain terminal couples to the cathode of said diode, and the anode of said diode and said gate
4 terminal couple to the negative terminal of said cell.

1 34. The battery of claim 21 further including a delay device coupled to said cell and said
2 transistor, said delay device slows the rate of change of voltage across said cell with changes in
3 current load on said cell.

1 35. The battery of claim 34 wherein said delay device comprises a resistor coupled to a
2 capacitor.

1 36. A battery cell protection circuit, comprising:
2 a current limiter capable of being coupled to a battery cell; and
3 a bypass device coupled in parallel with the current limiter and cell;
4 wherein the current limiter functions to limit current to the cell when the cell voltage
5 reaches a predetermined threshold.

1 37. The circuit of claim 36 wherein the current limiter comprises a transistor.

1 38. The circuit of claim 36 wherein the current limiter comprises an n-channel MOSFET.

1 39. The circuit of claim 36 wherein the current limiter comprises a p-channel MOSFET.

1 40. The circuit of claim 36 wherein the bypass device comprises a diode.

- 1 41. The circuit of claim 36 further including a delay element coupled to said current limiter to
2 delay the current limiting action of said current limiter when the cell voltage reaches the
3 predetermined threshold.

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